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(12) # EUROPEAN PATENT APPLICATION

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(54) **A method for tailoring oxygen precipitate particle density and distribution in silicon.**

(57) A wide precipitate-free-zone (PFZ) is formed at the surface of a semiconductor substrate and at the same time a high density of oxygen precipitate particles are produced beneath the surface PFZ layer by a two step annealing process involving a first cycle of very rapidly heating the wafers to a first high temperature and a second cycle of very slowly heating the wafers to a second high temperature.

EP 0 090 320 A1

A METHOD FOR TAILORING OXYGEN PRECIPITATE PARTICLE DENSITY AND DISTRIBUTION IN SILICON

The invention relates to a method for tailoring oxygen precipitate particle density and distribution in a silicon wafer, where the wafer is successively annealed at a first high temperature, at a low temperature and at a second high temperature.

The method deals especially with Czochralski grown silicon wafers. The precipitation of oxygen has become an important parameter in describing the interaction between device processing yields and the starting silicon substrate.

It has been known that Czochralski silicon wafers include interstitial oxygen which may precipitate and form microdefects during processing at elevated temperatures. Such microdefects may be either beneficial or detrimental to device performance.

To achieve beneficial results, the precipitation and associated defects must be confined to the bulk of the wafer leaving a region adjacent to the wafer surface free of microdefects. It is known that the oxygen precipitates formed in the bulk of silicon wafers work as internal gettering centers.

The concept of internally gettering detrimental contamination elements such as Fe, Ni, Cu and Au is described in IBM Technical Disclosure Bulletin, Vol. 19, No. 4, September 1976, page 1295. This article reports that defects in the silicon wafer are diffused internally by suitably controlled high temperature annealing, which

makes it possible to obtain a surface layer free from defects while keeping a useful gettering effect in the bulk of the wafer. When these defects are located in the surface layer or close to the surface layer, they are known to cause pipe phenomenon or leakage currents.

"Influence of Precipitate Size and Capillarity Effects on the Surface Denuded Zone In Thermally Processed Cz-Silicon Wafers", by R. W. Series et al., published in "Semiconductor Silicon" Electro-Chemcal Society, 1981, pages 304-312 reports that controlled denuded zones with bulk intrinsic gettering centers can be produced by a two stage process involving first a high temperature (e.g., 1150°C) then a low temperature (e.g., 750°C) heat treatment. However, if a straight 750°C anneal is used, the times will be prohibitively long and the number of particles will be low.

"Denuded Zone and Microdefect Formation in Czochralsky-Growth Silicon Wafers by Thermal Annealing" by K. Kugimiya et al., published in "Semiconductor Silicon" Electro-Chemical Society, 1981, pages 294-303, reports a two-step anneal to obtain a defect-free zone at the surface and a precipitate particle density of approximately $10^{10}/cm^3$ beneath this layer. The high temperature cycle mentioned is four hours at 1100°C to 1200°C followed by a 650°C-800°C nucleation anneal for seventy hours and then a 1000°C-1100°C six hour anneal to grow the precipitates. The observed particle densities are too low and the process is too long.

"The Nucleation and Growth of Oxide Precipitates in Silicon" by H. F. Schaake et al., published in "Semiconductor Silicon" Electro-Chemical Society, 1981, pages

273-281 reports using a 1000°C half an hour treatment to dissolve pre-existing nuclei. They then anneal forty-eight hours at 450°C to nucleate new precipitates and then anneal 120 hours at 750°C to grow them. The observed precipitate particle densities were $10^{12}/cm^3$. The process is too long to be practical for manufacturing.

U.S. Patent No. 4 220 483 teaches that the gettering effect in the bulk of semiconductor bodies is increased by heating the bodies prior to device processing to a temperature of from 750°-900°C for from 1-8 hours in order to generate oxygen precipitates in the form of clusters. Our experimentation in this temperature range indicates that the particle density will be too low for effective strengthening of the wafer.

IBM Technical Disclosure Bulletin, Vol. 19, No. 12, May 1977, pp. 4618-4619 reports that heating semiconductor wafers at temperatures of about 1000°C for 4 to 6 hours in a dry oxygen or inert atmosphere causes out-diffusion of oxygen from the semiconductor surface so that a defect-free surface layer is formed.

Control of oxygen precipitation by annealing silicon wafers has been extensively studied. To date, however, no practical sequence of anneal cycles has been discovered which will remove pre-existing oxygen clusters, out-diffuse oxygen from the wafer surface and thus cause uniform, dense precipitation beneath this surface layer to allow impurity gettering by precipitation-induced defects.

It is the object of the present invention to provide a method for forming a wide precipitate free zone at the

surface of a semiconductor substrate with a high density of precipitate particles underneath, within a relatively short time.

This object is achieved by a method as defined at the beginning of this specification having the features of the characterizing part of claim 1.

In accordance with the present invention, a wide precipitate-free-zone (PFZ) is formed at the surface of a semiconductor substrate and at the same time a high density of precipitate particles are produced beneath the surface PFZ layer by the two step annealing process involving first a high temperature cycle and then a low temperature cycle.

The purpose of the high temperature cycle is twofold, that is, to reduce the number of pre-existing oxygen clusters by dissolution and to out-diffuse the oxygen as the first step in the formation of precipitate-free zone. The high temperature cycle can be carried out at any temperature above 1000°C, the upper limit being set by the melting point of the silicon of about 1415°C. Practically, this temperature should be chosen to be as high as possible without introducing plastic deformation of the wafers. It was found experimentally that this can be realized for 82.5 mm wafers around 1100°C. A further consideration is the softening of the SiO_2 glassware above about 1150°C. It is important that the wafers are rapidly heated to the high temperature, that is, at a rate in excess of 10°C/minute. Preferably, the wafers are brought to the high temperature by rapid insertion into the furnace tube which is already at

1100°C. The wafers are held at the high temperature for about four hours and ramped back down to a lower temperature such as 800°C at which point they are removed from the furnace.

The width of the PFZ depends on the oxygen profile formed in this high temperature out-diffusion step. It was found that four hours at 1100°C is appropriate for obtaining PFZ widths in excess of 15μm.

It is recognized that dissolution of the pre- existing precipitates and clusters is insured by the rapid heat-up at a rate in excess of 10°C/minute. When lower heat-up rate is used, precipitation of oxygen begins, which is detrimental to the first purpose of the high temperature cycle, that is, to reduce the number of pre-existing oxygen clusters by dissolution.

The process proceeds to the low temperature cycle. The purpose of this portion of the process is to precipitate the oxygen and form a high density of very small precipitate particles. These small particles, however, must be large enough to survive the initial device hot processes. The strategy followed is to nucleate the precipitates at a low temperature and then grow them to such a size as to permit survival of a subsequent heat treatment such as 925°C, two hour anneal for oxidation step. The wafers are annealed at a low temperature of the range of 400°C to 500°C, preferably at 450°C for about four hours. This annealing yields about 1×10^{15} donor clusters. It is assumed that each cluster size has a temperature range in which it is stable. If this temperature range is exceeded, the cluster will dissolve.

After the low temperature anneal, the wafers are very slowly heated to a second high temperature in the range of 750°C to 1000°C, at a rate lower than 2°C/minute. If higher ramp rate is used, it will result in much lower precipitate particle density. The wafers are annealed at the second high temperature so that the precipitated particles nucleated during the low temperature anneal grow to a size which will insure their survival in subsequent device processing. The particle growth is a diffusion controlled mechanism and the growth temperature must be high enough to give adequate mobility to the oxygen atoms. Since the wafers have to be heated very slowly, it is practical to heat up the wafers to a temperature in the range from 750°C to 850°C at a very low rate and after a pause at this temperature the wafers may be heated up to a temperature of from 900°C to 1000°C at a higher rate, which is the temperature of the first hot process in the device line, to insure that the particles will not be dissolved in the subsequent process.

Other advantageous embodiments of the inventive method are disclosed in the subclaims.

The invention will become more apparent from the following detailed description taken in conjunction with the accompanying drawings.

Brief Description of Drawing

Fig. 1 is the temperature-time diagram of the high temperature cycle in one example of the invention.

Fig. 2 is the temperature-time diagram of the low temperature cycle in one example of the invention.

Fig. 3 is the temperature-time diagram of the low temperature cycle in another example of the invention.

Fig. 4 is the microscopic photograph of the cross section of a wafer which was processed with the method of the present invention.

Fig. 5 is the microscopic photograph of the cross section of a wafer which was processed with a conventional process.

Semiconductor wafers of 82.5 mm in diameter are rapidly heated up to 1100°C by rapid insertion of the same into the furnace tube which is already at 1100°C. Recovery of the furnace temperature occurs within two minutes of insertion of the wafers. In the case of the 100 mm diameter wafers, it is preferable to heat them up by rapid insertion into the furnace at 1000°C and immediately ramping to 1100°C at 10°C/minute to avoid the problems of plastic deformation which causes both peripheral slip and center slip.

The wafers are held at 1100°C for four hours for oxygen out-diffusion and ramped back to 800°C at 5°C/minute at which point they are removed from the furnace. Fig. 1 shows this high temperature cycle.

The process now proceeds to the low temperature cycle. After being annealed at 450°C for four hours, the

wafers are slowly heated to 800°C at a rate of 0.84°C/minute and kept at this temperature for two hours. So as to insure that the precipitate particles survive in subsequent device processing, the wafers are annealed at 925°C for two hours, which is the temperature of the first hot process in the device manufacturing line. The wafers are now ramped down to 800°C and removed from the furnace.

This low temperature cycle is illustrated in Fig. 2. The total cycle time of the low temperature cycle is sixteen hours.

Another mode of the low temperature cycle is illustrated in Fig. 3. Pieces were cleaved from the wafers and they were beveled at 5° on a ground glass plate using silica gel polishing slurry which is widely used for polishing silicon wafers. The beveled samples were etched for two minutes to reveal the oxygen precipitates. It was found by optical microscopy that the precipitate free zone was in excess of 16 µm and the precipitate particle density was larger than $10^{12}/cm^3$. The microscopic photograph of the cross section of the wafer is shown in Fig. 4. In contrast, a similar microscopic photograph of a beveled cross section of a wafer which was processed with a conventional semiconductor device manufacturing process is shown in Fig. 5. The precipitate free zone at the surface of the wafer is shallow and the oxygen precipitates are located close to the surface layer, which may cause pipe phenomenon or leakage currents thereby resulting in low yield of large scale integrated circuit devices.

C L A I M S

1. Method for tailoring oxygen precipitate particle density and distribution in a silicon wafer, where the wafer is successively annealed at a first high temperature, at a low temperature and at a second high temperature,

characterized in that the wafer is heated to said first high temperature at a rate higher than 10°C/minute and to said second high temperature at least during the first part of the temperature increase at a rate lower than 2°C/minute.

2. The method of claim 1 wherein said low temperature is between 400°C and 500°C.

3. The method of claim 2 wherein said second high temperature is between 750°C and 1000°C.

4. The method of claim 3 wherein said first high temperature is between 1000°C and 1400°C.

5. The method of claim 4 wherein said wafer is heated up to said first high temperature by inserting said wafer into a furnace which is already substantially at said first high temperature.

6. The method of claim 5 wherein said wafer is kept at said first high temperature for approximately four hours.

7. The method of claim 4 wherein said wafer is ramped down from said first high temperature to approximately 800°C and removed from the furnace.

8. A method for tailoring oxygen precipitate particle density and distribution in a silicon wafer, comprising the steps of:

heating the silicon wafer to a first high temperature at a rate higher than 10°C/minute,

keeping said wafer at an elevated temperature for a period sufficient to allow outdiffusion of oxygen,

annealing said wafer at a low temperature,

heating said wafer to a temperature in the range of 750°C to 850°C at a rate lower than 2°C/minute, and

heating said wafer to a temperature in the range of 900°C to 1000°C at a higher rate.

9. A method for tailoring oxygen precipitate particle density and distribution in a silicon wafer, comprising the steps of:

heating the silicon wafer to a first high temperature at a rate higher than 10°C/minute,

keeping said wafer at an elevated temperature for a period sufficient to allow outdiffusion of oxygen,

annealing said wafer at a low temperature,

heating said wafer to a second high temperature of approximately 650°C at a rate lower than 2°C/minute,

keeping said wafer at said second high temperature for a time sufficient to grow precipitate particles, and

heating said wafers to a third high temperature in the range of 750°C to 850°C at a higher rate.

10. The method of claim 9 wherein the time sufficient to grow precipitate particles is about sixteen hours.

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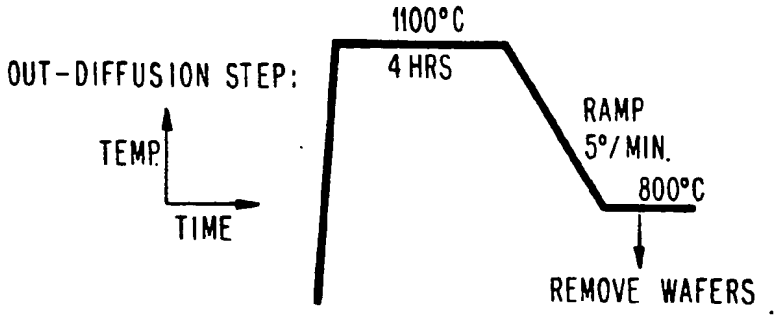

FIG. 1

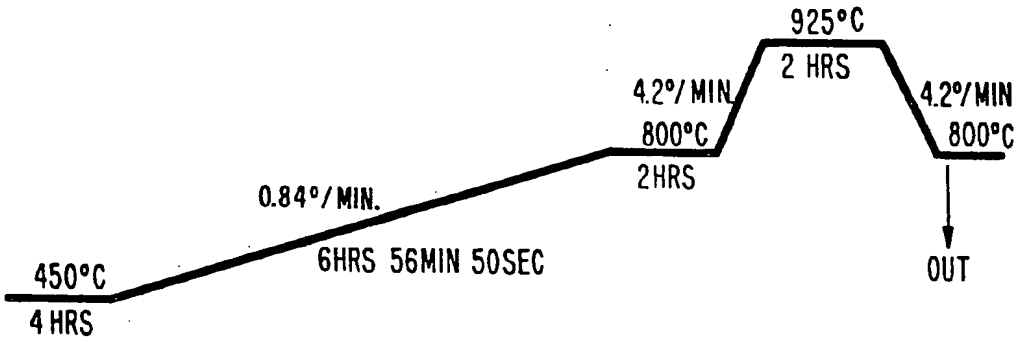

FIG. 2

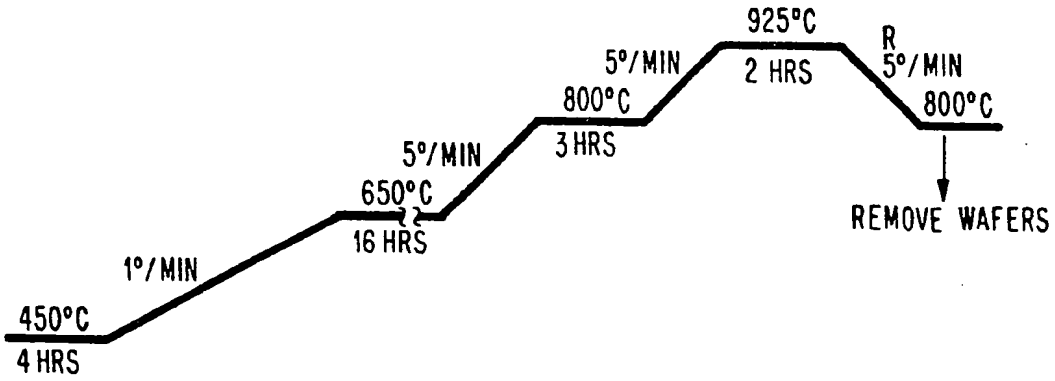

FIG. 3

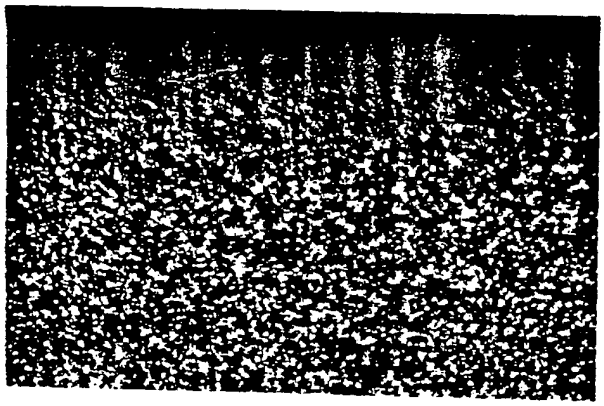

FIG. 4

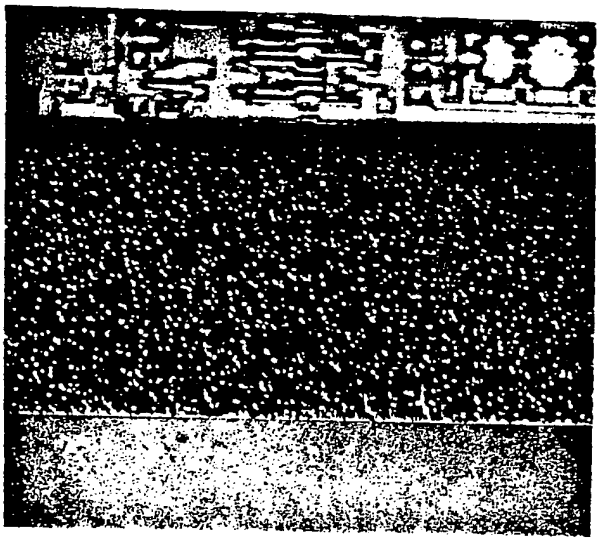

FIG. 5

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EUROPEAN SEARCH REPORT

Application number
0090320

EP 83 10 2805

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
A	GB-A-2 080 780 (THE SECRETARY OF STATE FOR DEFENCE) -----		C 30 B 33/00 C 30 B 29/06

TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

C 30 B 33/00
C 30 B 29/06

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	04-07-1983	BRACKE P.P.J.L.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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L : document cited for other reasons

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